Value Communications Appliance Reference Schematics

Table of Contents

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Revision History

03/14/2000 Revision A0 -- Initial release.

These schematics are preliminary and subject to change without notice.

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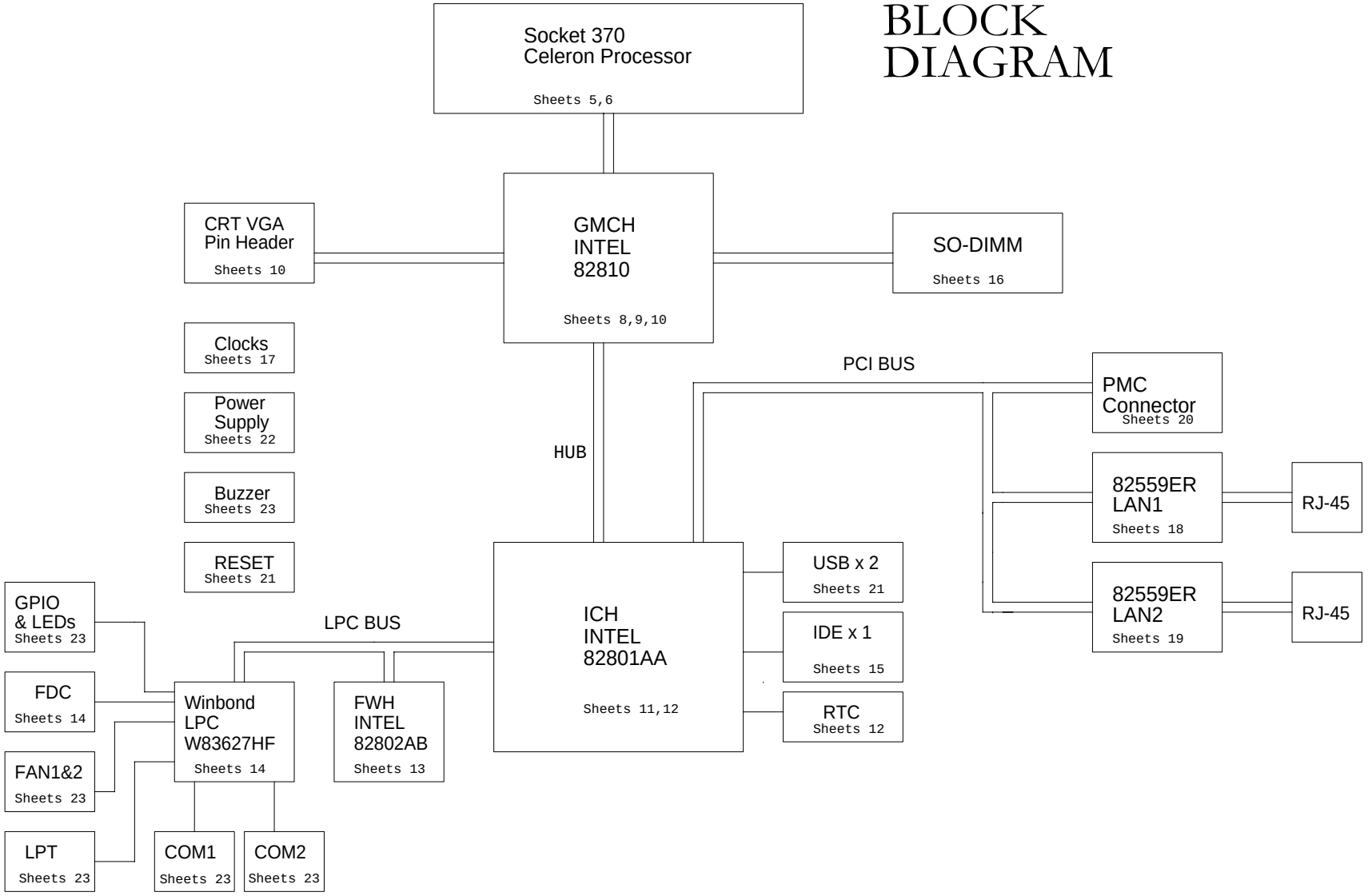
Title: Value Communications Appliance Reference Schematics		
Title		
Size: B	Document Number: 0754 Value Communications Appliance	Rev: A0
Date: Tuesday, July 18, 2000	Sheet 1 of 23	

BLOCK DIAGRAM



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Title	Value Communications Appliance Reference Schematics Block Diagram	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 2 of 23	

General Board Design Requirements

>> PCB must be routed using six (6) layers, with the following stackup:

Layer 1: Signal, V1P5,V1P8, V2P5, and V5P0 Busses
Layer 2: GND
Layer 3: Signal
Layer 4: Signal
Layer 5: Split Power Plane -- V3P3 Plane, V2P0 Island
Layer 6: Signal

>> Right angle traces must not be used.

>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.

>> Trace impedance must be 65 ohms, +/- 10%

>> Total board thickness must be .062".

>> Board material must be FR-4.

>> GND layers must not be split.

>> Top and bottom (outer) layers must be no less than 1/2 oz copper before plating, inner layers must be 1 oz copper.

>> Series terminating resistors must be kept as close to the driving pin as possible.

>> Daisy chain signals going to more that on point, do not use stubs.

>> Unless otherwise noted, all signal traces must be between 5 and 6 mil width.

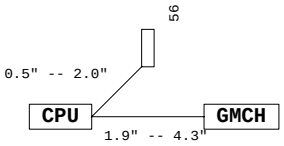
>> Unless otherwise noted, minimum space between traces is 15 mils, including adjacent layers.

>> Specific routing reqirements are included throughout schematic sheets.

>> One registration target must be included on each corner of the board.

CPU Routing Requirements

>> Route all GTL traces between CPU and GMCH as shown in the diagram to the right.



>> Route all traces between CPU and GMCH on a layer adjacent to a ground plane (preferably bottom layer), without layer changes.

>> All traces between CPU and GMCH should differ in length by no more than 1000 mils.

>> Minimum space between traces is 15 mils (unless otherwise noted), this includes adjacent signal layers.

>> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing must be less than 250 mils.

>> The following signals require 25 mil spacing from other traces, including adjacent layers.

HA#[31:3], HD#[63:0], BREQ#0, ADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, A20M#, FLASH#, IGNNE#, INIT#, INTR, NMI, PWR_OK_2P5, SMI#, CPUSLP#, STPCLK#, 100/66#, FERR#, HRESET#, HREQ#[4:0], RS#[2:0], THERMD[P:N], CPU_GTL_REF[7:0], PLL[2:1], (TCK,TMS,TDI, TDO, TRST#, PRDY#, PREQ#).

>> Route THRMDP and THRMDN close together as a pair (no more than 250 mil difference in length), on same layer, in parallel, and 25 mils min from any other trace.

>> Route CPU_GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.

>> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.

Clock Specific Routing Requirements

>> A clock trace must not alternate layers.

>> A clock trace must be separated by a minimum of 25 mils from any other trace, including serpentines, 11 mils is OK when going betwen pins or balls.

>> The CPU clock length must be between 1" and 9", and 460 mils shorter than the GMCH clock. The GMCH_3V66 clock and ICH_3V66 clock must be matched in length. All PCI clocks must be matched in length, except for the PMC clock which must be 2" shorter than all other PCI clocks.

>> SDRAM_CLK[1:0] must be matched in length, and between 1" and 3" in length.

>> DCKL_WR, from the SDRAM clock driver to the GMCH, must be between 3.5" and 5.5" in length, and 2.5" longer than SDRAM_CLK[1:0].

IDE Specific Routing Requirements

>> Place IDE conector within 8" of ICH.

Power Supply Specific Routing Requirements

>> All unrelated signals and power planes must be kept away from the switching circuits.

>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.

>> See the Power Supply schematic sheet for complete restrictions.

Memory Bus Specific Routing Requirements

>> Minimum trace width is 5 mils.

>> Minimum space between traces is 10 mils, this includes adjacent signal layers.

>> Minimum space between memory traces and other types of traces is 25 mils, this includes adjacent signal layers.

>> Memory address, data, and control lines must be routed as separate groups and treated as different signal types.

>> The MD, DQMA, CSA#, SRAS#, SCAS#, WE_A#, and MA signals (between GMCH and SODIMM) must be between 1" and 3" in length, matched to within 600 mils.

Memory Bus GROUPS -- SO-DIMM Names

>> Address Signals: MAA[13:0]

>> Data Signals: MD#[63:0]

>> Control Signals:

SMBDATA, SMBCLK, CSA[1:0]#, WE_A#, SCAS#, SRAS#

PCI Bus Specific Routing Requirements

>> PCI bus max length must be less than 6".

PCI Bus GROUPS

>> Address/Data Signals: AD[31:0]

>> Control Signals:

C/BE[3:0]#, REQ[4:1]#, GNT[4:1]#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

HUB Bus GROUPS

>> Address/Data Signals: HL[10:0]

>> Control Signals: HLSTB,HLSTB# (differential strobe pair).

>> HL[10:0] should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. The maximum trace length for the hub interface data signals is 7". These signals should each be matched within .1"" of the HLSTB and HLSTB# signals.

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Title: Value Communications Appliance Reference Schematics
Routing Guidelines/Restrictions

Size	Document Number	Rev
B	0754	A0

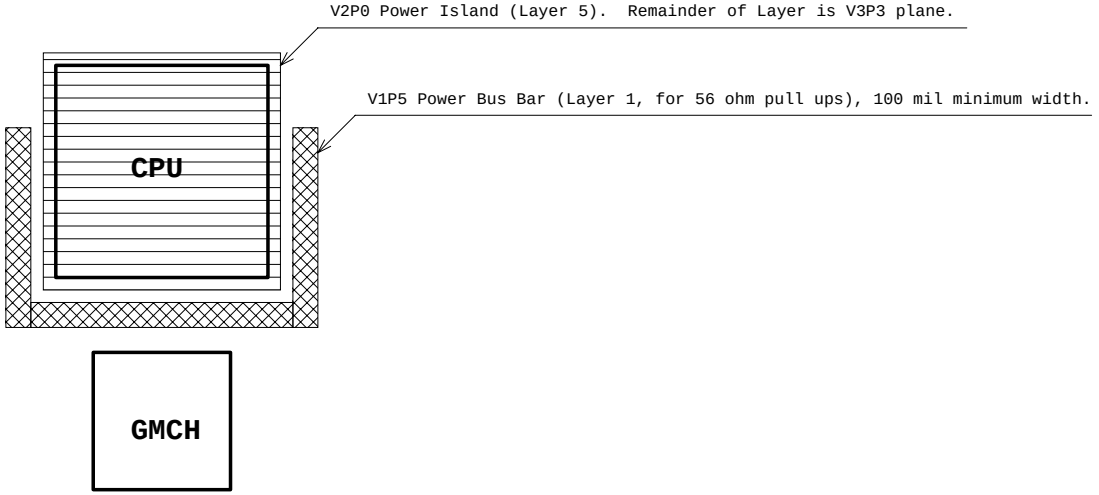
Date: Tuesday, July 18, 2000 Sheet 3 of 23

General Placement Requirements

>> Place major components and connectors as shown in the Mechanical drawings.

CPU/GMCH Specific Routing Requirements.

>> Rotate the CPU and GMCH chips so as to minimize the length of the connections between the two, and place as shown in the diagram below:



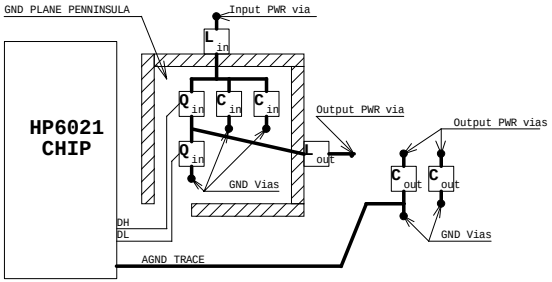
>> The V2P0 power supply must not be layed over the V2P0 power island. The power supply feed to the power island must be the maximum practical width.

>> The V1P5 power supply must not be layed over the V1P5 power island. The power supply feed to the power island must be the maximum practical width.

>> The V2P0 power island depiction above, is approximate, and must be large enough to fully encompass the entire CPU as well as any component that connects to the V2P0 supply.

Power Supply specific Routing Requirements.

>> The diagram below depicts the placement requirements for the SC1164 switching regulator circuits. A GND plane penninsula is used to contain the high current and noisy switching components. All of the bold traces and vias shown have high current and low impedance requirements. These trace widths should be 100 mils minimum. The channel which connects the GND penninsula to the main GND plane must be 500 mils in width.



>> No other signals may be routed underneath the GND plane penninsula.

>> No other power planes may exist underneath the GND plane penninsula.

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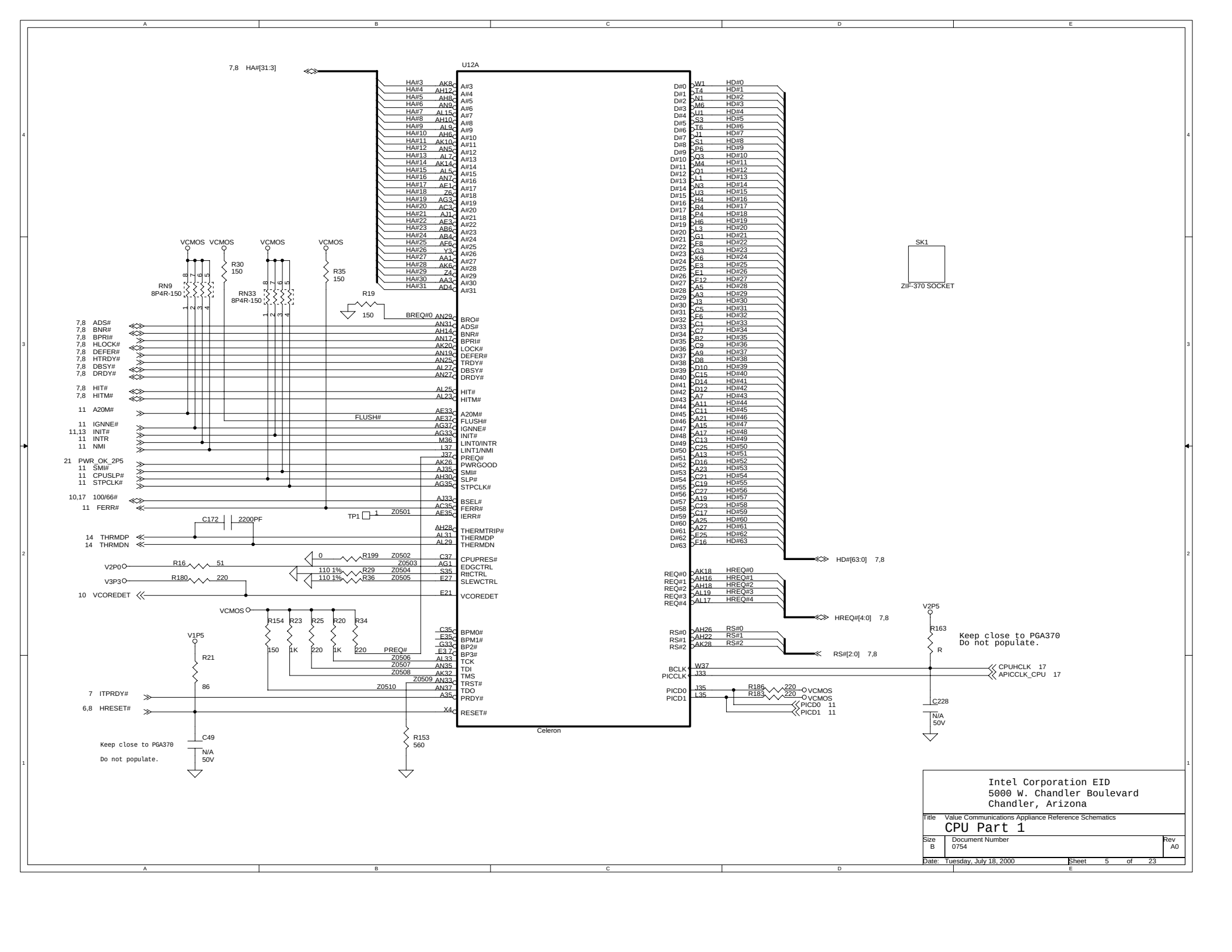
Title: Value Communications Appliance Reference Schematics		
Routing Guidelines/Restrictions		
Size: B	Document Number: 0754	Rev: A0
Date: Tuesday, July 18, 2000	Sheet 4 of 23	



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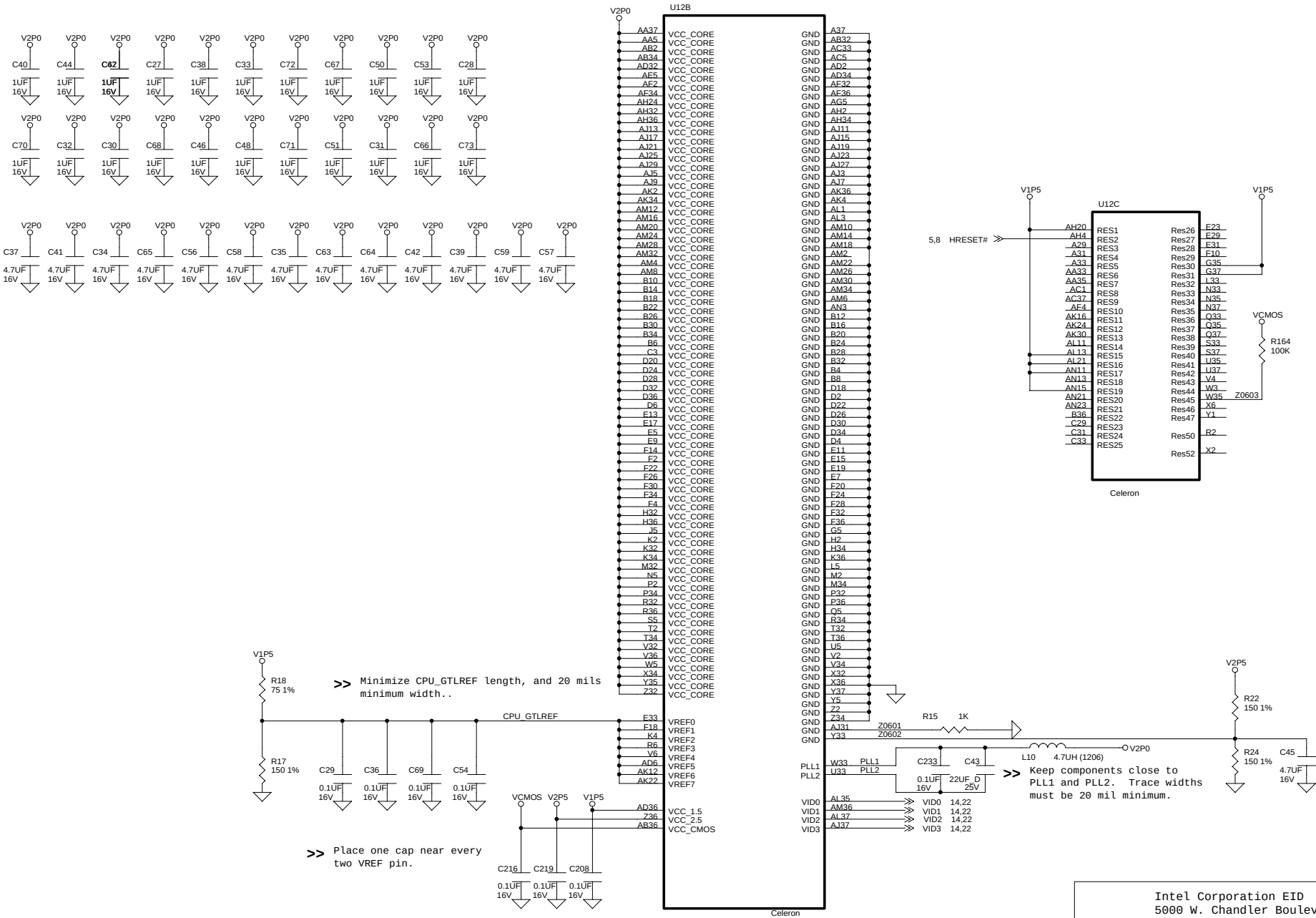
Title	Value Communications Appliance Reference Schematics CPU Part 1	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 5 of 23	



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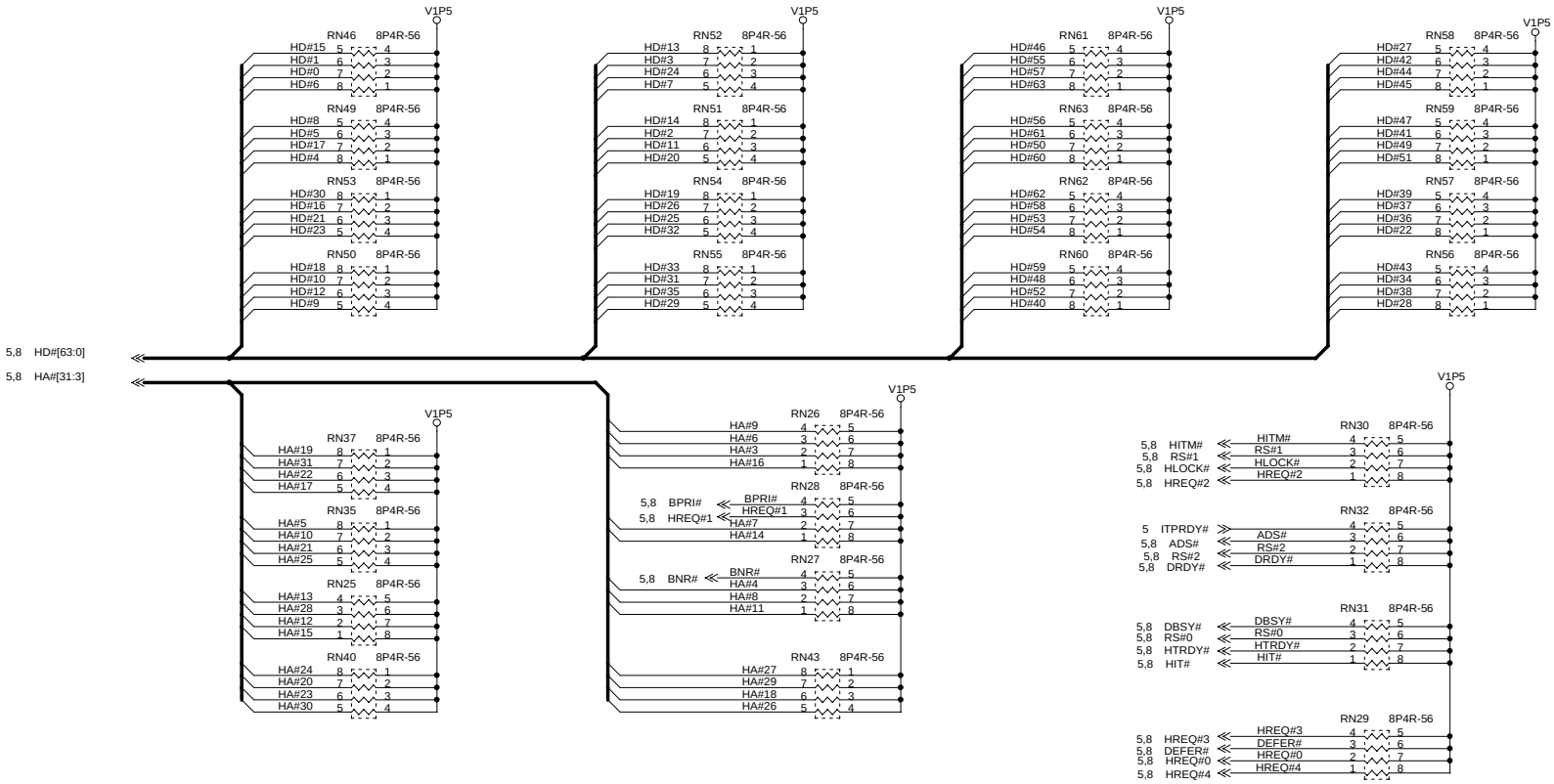
Title: Value Communications Appliance Reference Schematics

CPU Part Two

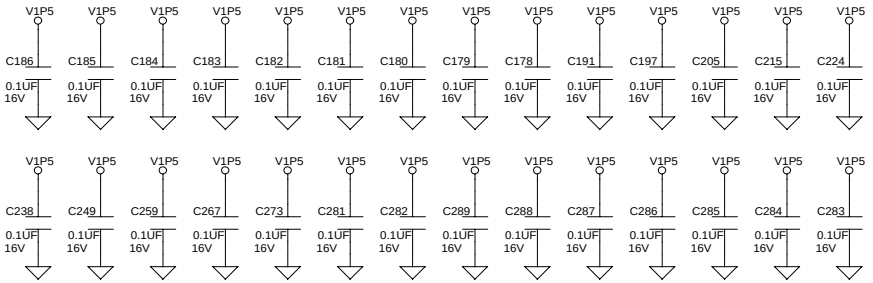
Size	Document Number	Rev
B	0754	A0

Date: Tuesday, July 18, 2000 Sheet 6 of 23

GTL+ TERMINATION RESISTORS



>> Place one CAP for every resistor pack.



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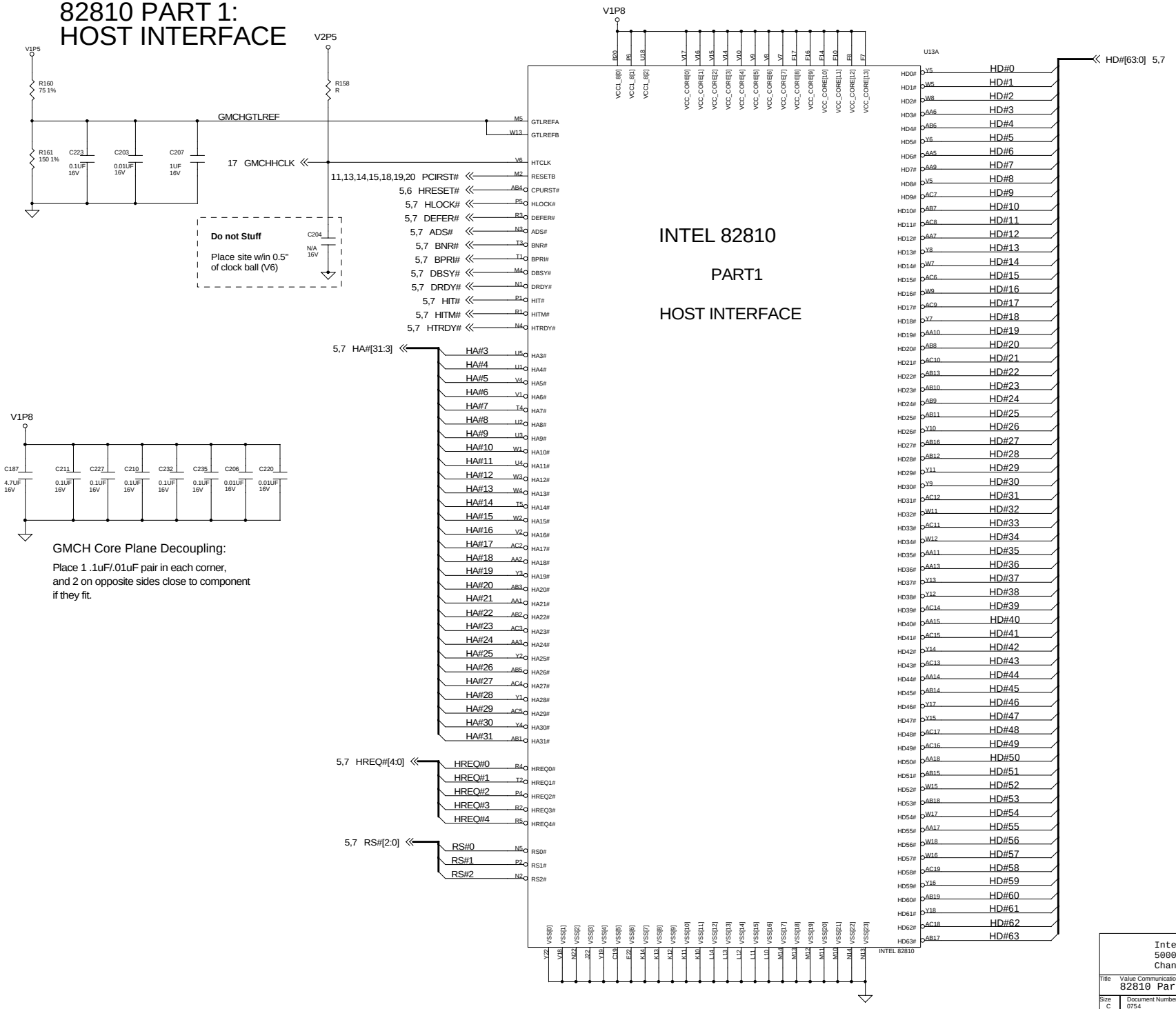
Title	Value Communications Appliance Reference Schematics GTL+ Termination	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 7 of 23	

82810 PART 1: HOST INTERFACE



GMCH Core Plane Decoupling:

Place 1 .1uF/.01uF pair in each corner, and 2 on opposite sides close to component if they fit.

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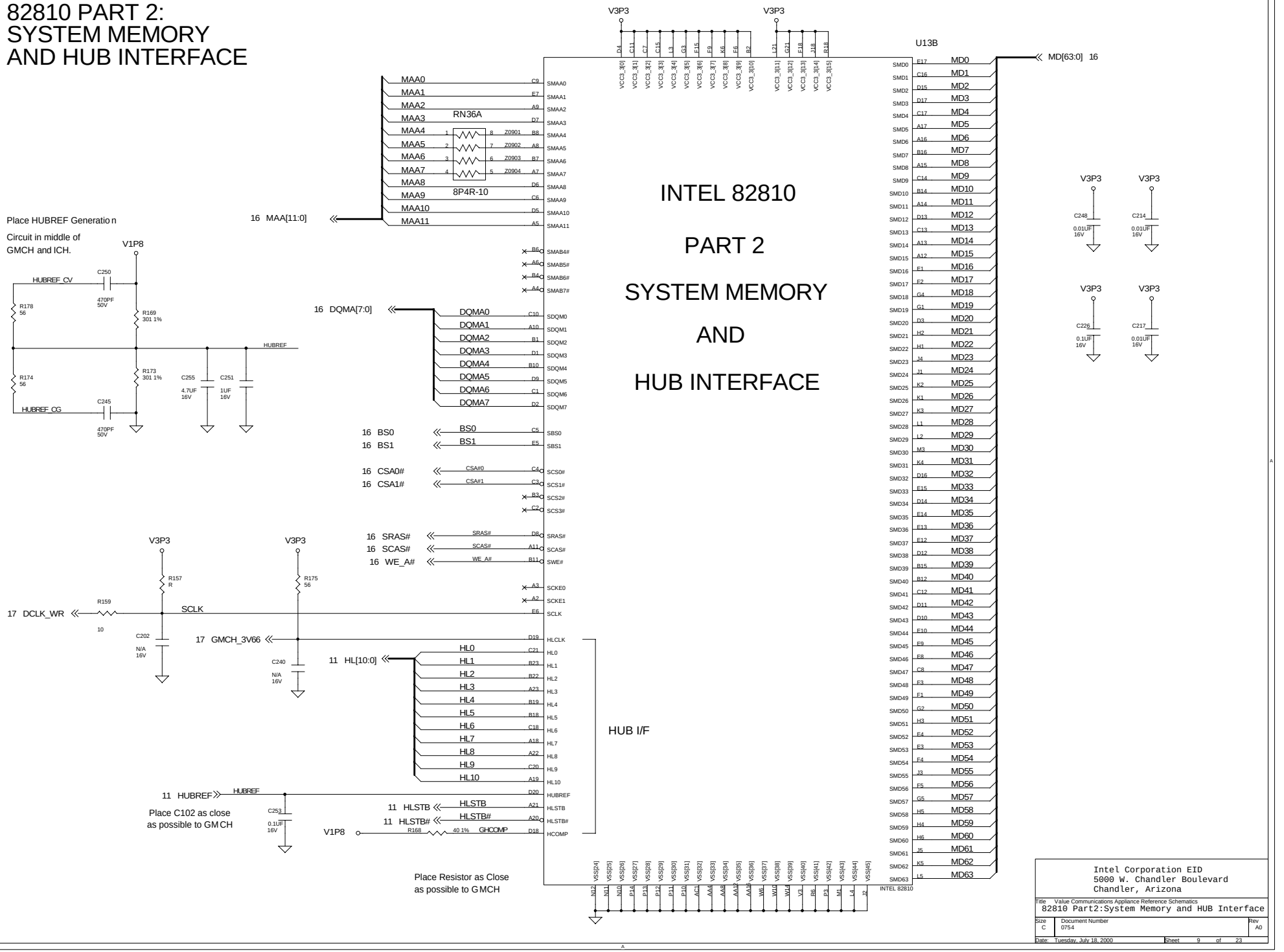
Title	Value Communications Appliance Reference Schematics 82810 Part1:Host Interface	
Size C	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 8 of 23	

82810 PART 2: SYSTEM MEMORY AND HUB INTERFACE



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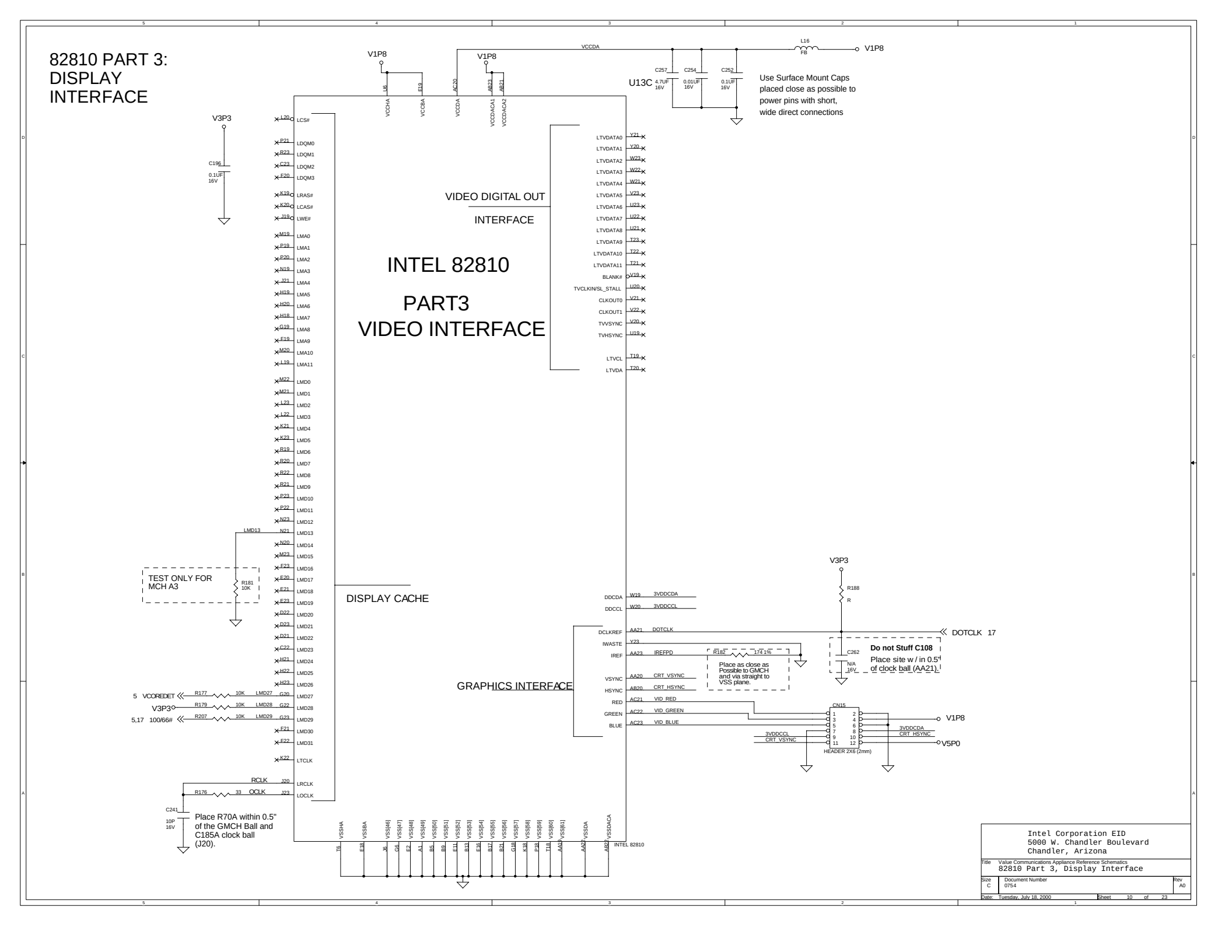
Title: Value Communications Appliance Reference Schematics 82810 Part2:System Memory and HUB Interface	
Size: C	Document Number: 0754 — Rev: A0
Date: Tuesday, July 18, 2000	Sheet 9 of 23

82810 PART 3: DISPLAY INTERFACE



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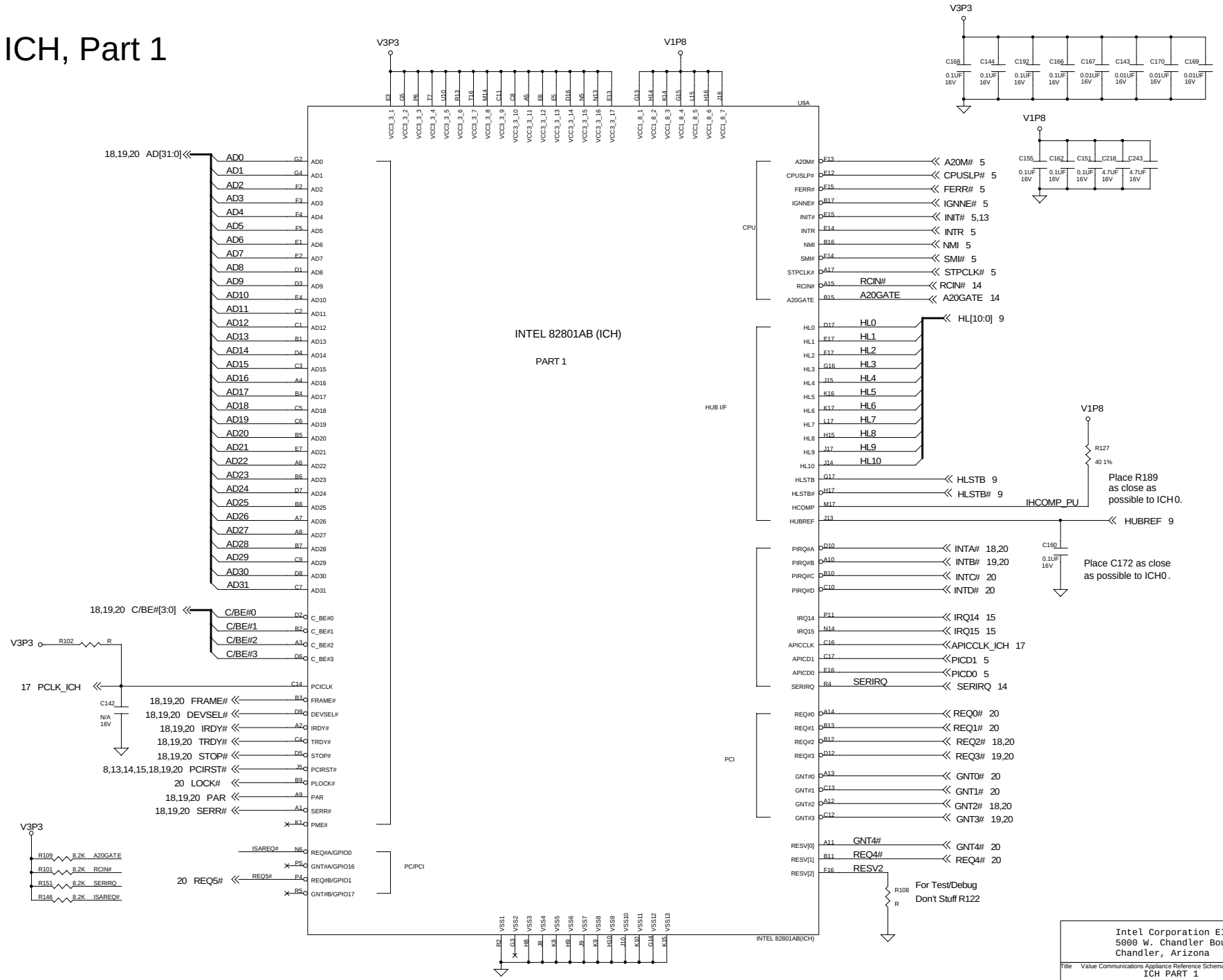
Title	Value Communications Appliance Reference Schematics 82810 Part 3, Display Interface	
Size C	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 10 of 23	

ICH, Part 1



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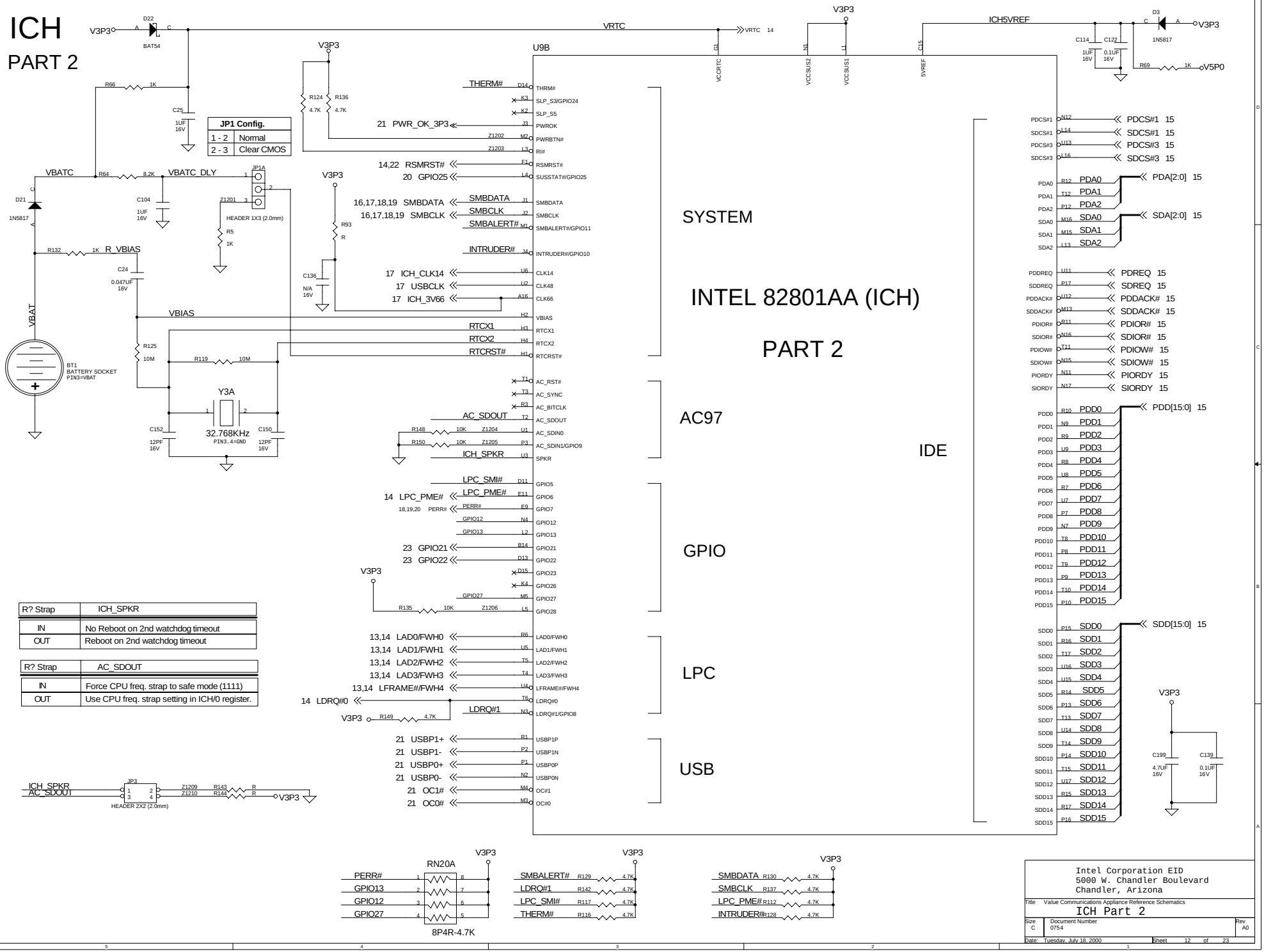
Title	Value Communications Appliance Reference Schematics ICH PART 1	
Size C	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 11 of 23	

ICH
PART 2


U9B
SYSTEM
AC97
GPIO
LPC
USB
IDE
INTEL 82801AA (ICH)
PART 2
JP1 Config.
1 - 2 Normal
2 - 3 Clear CMOS
R? Strap ICH_SPKR
IN No Reboot on 2nd watchdog timeout
OUT Reboot on 2nd watchdog timeout
R? Strap AC_SDOUT
IN Force CPU freq. strap to safe mode (1111)
OUT Use CPU freq. strap setting in ICH/0 register.
RN20A
8P4R-4.7K
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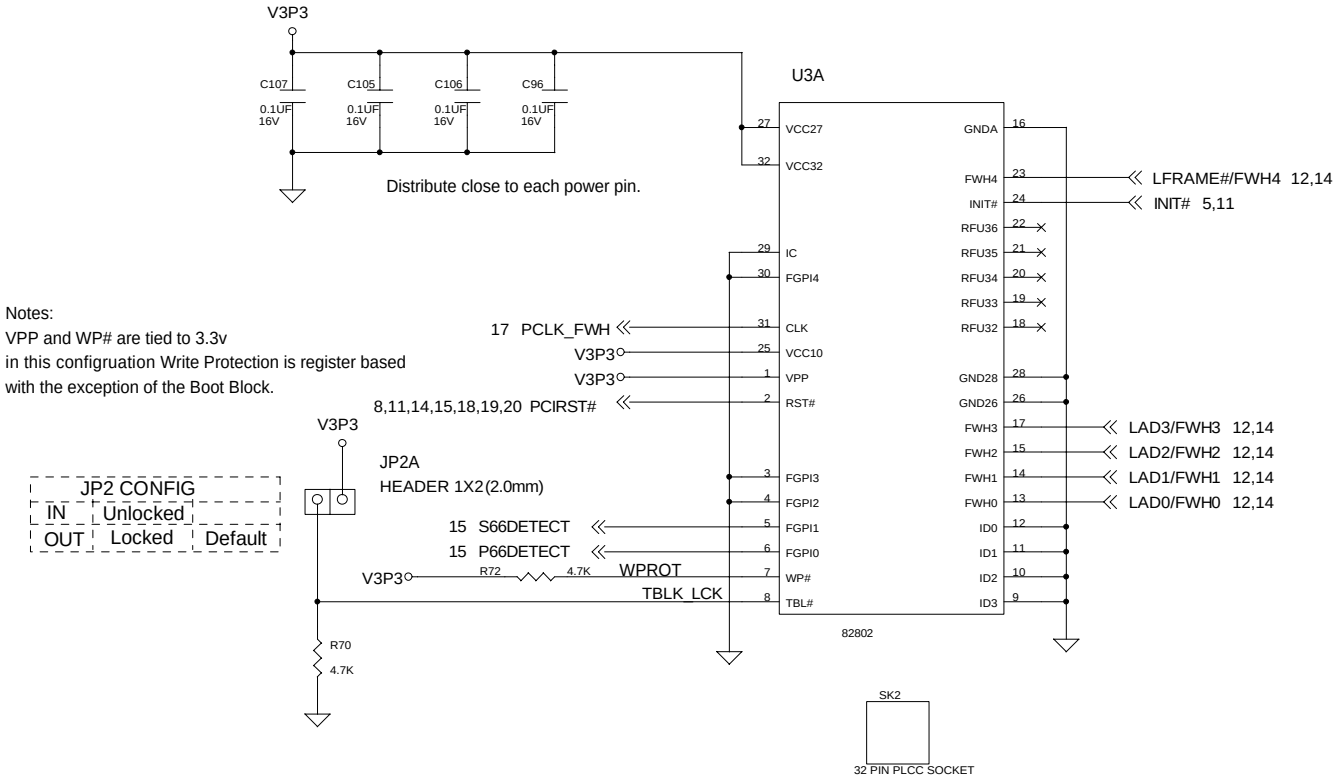
Value Communications Appliance Reference Schematics
ICH Part 2
Document Number 0754
Rev A0
Date: Tuesday, July 18, 2000
Sheet 12 of 23

FirmWare Hub (FWH)



Notes:
VPP and WP# are tied to 3.3v
in this configuration Write Protection is register based
with the exception of the Boot Block.

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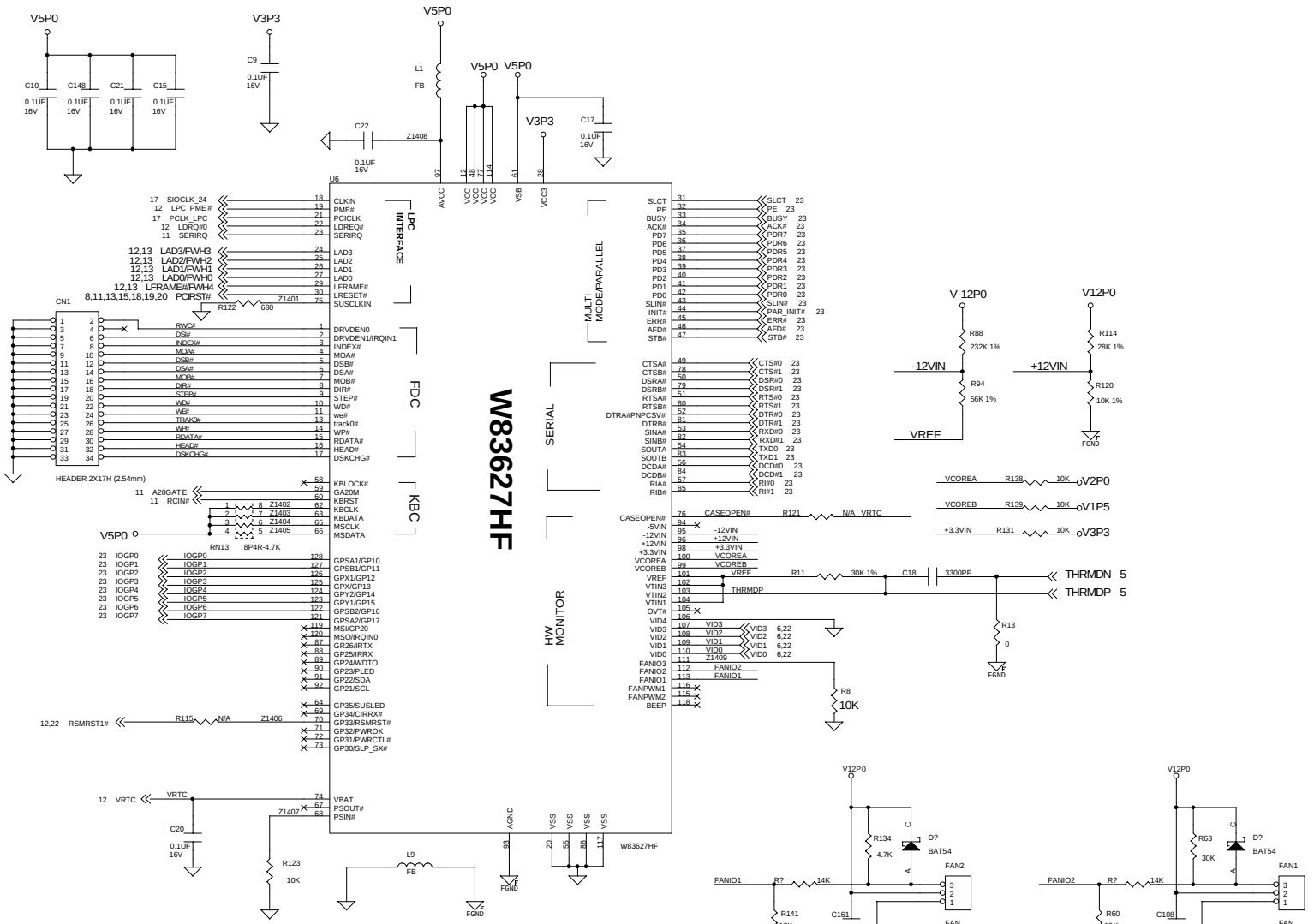
Title	Value Communications Appliance Reference Schematics FirmWare Hub (FWH)	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 13 of 23	


W83627HF
LPC INTERFACE
FDC
KBC
SERIAL
MULTI MODE/PARALLEL
HW MONITOR
V5P0
V3P3
V12P0
V-12P0
-12VIN
+12VIN
VREF
THRMDN 5
THRMDP 5
FAN1
FAN2
FAN
BAT54
HEADER 2X17H (2.54mm)
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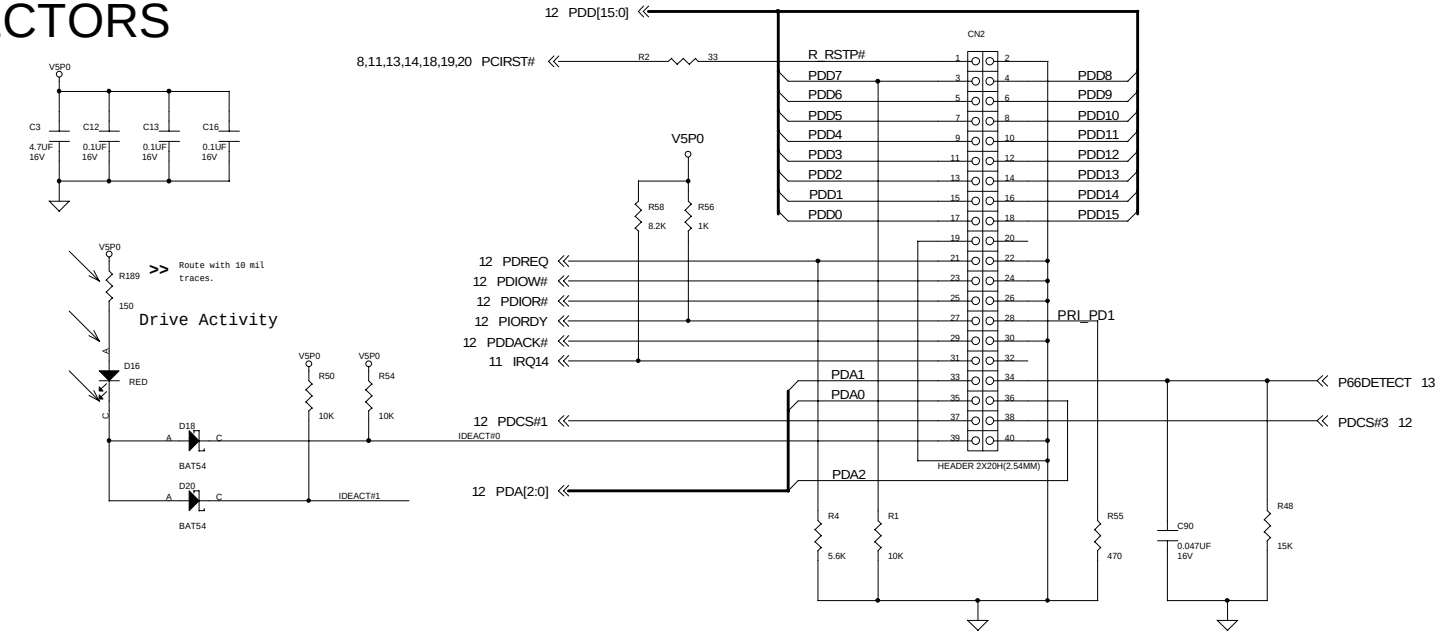
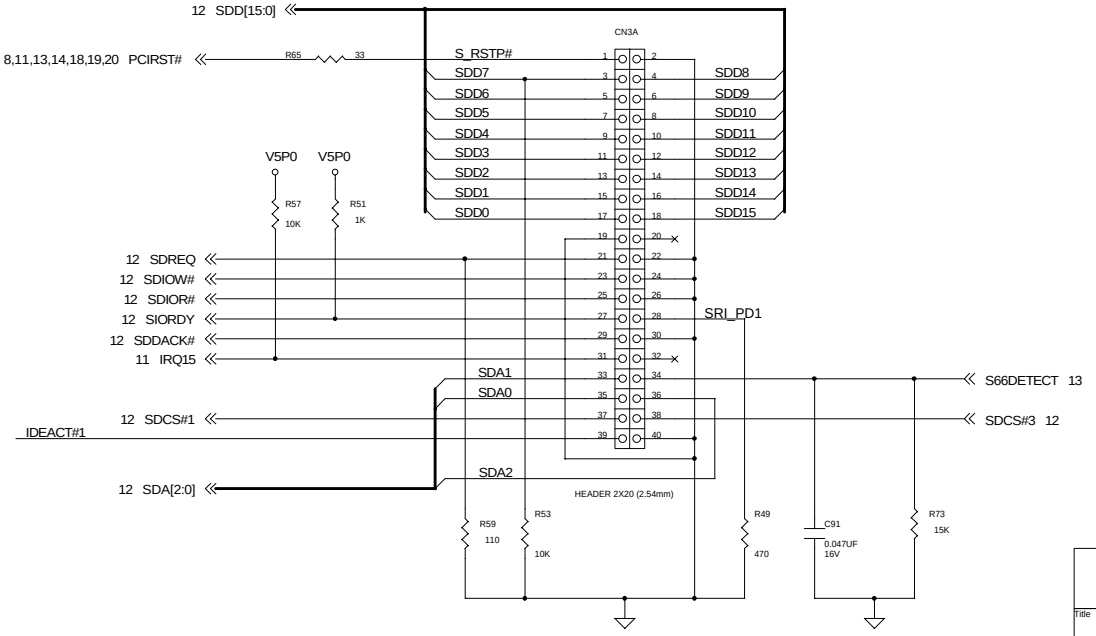
Chandler, Arizona
Value Communications Appliance Reference Schematics
Super I/O (LPC)
Document Number 0754
Rev A0
Tuesday, July 18, 2000
Sheet 14 of 23

ULTRA ATA33/66 IDE CONNECTORS



IDE CONN



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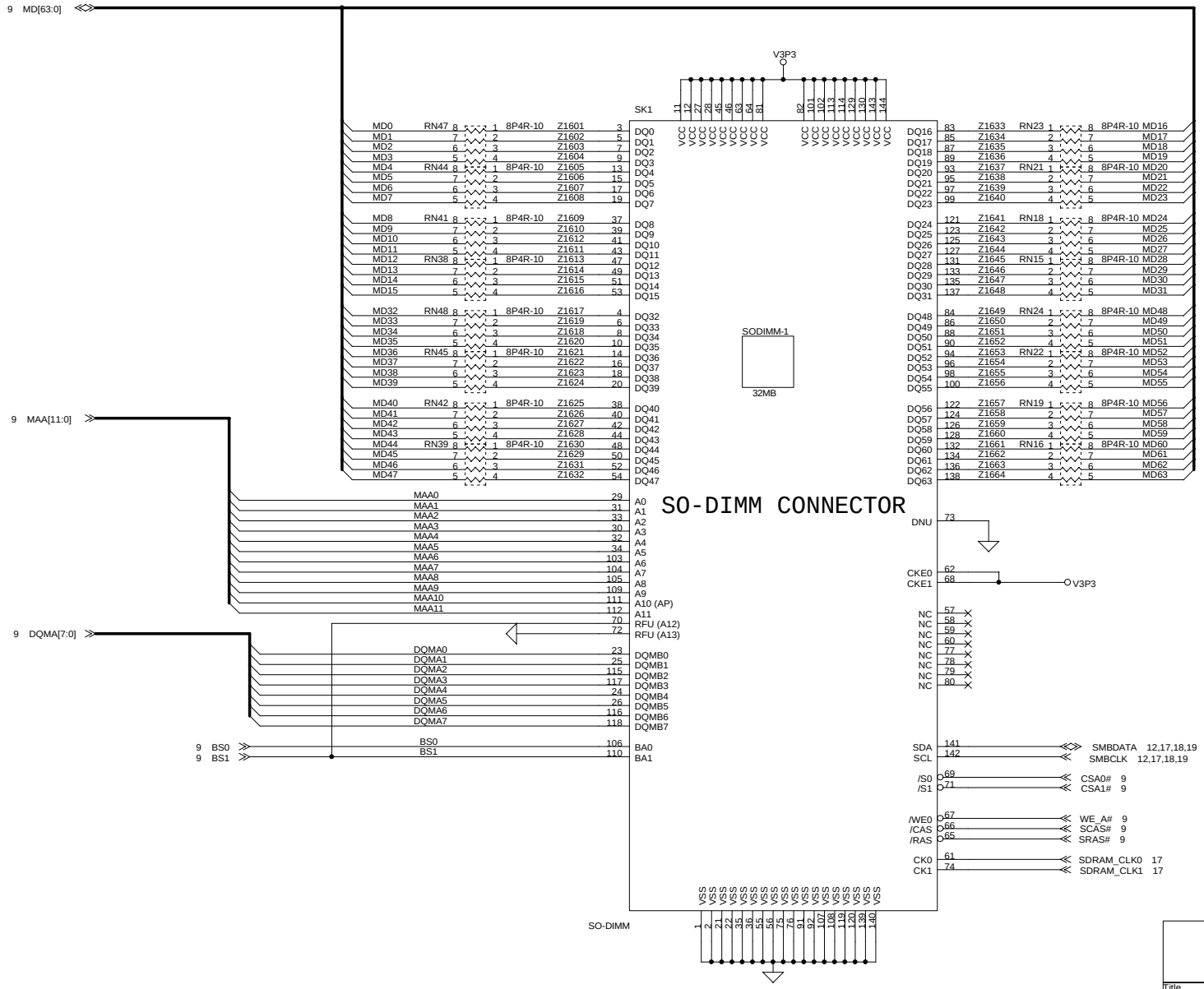
Title	Value Communications Appliance Reference Schematics	
	ULTRA ATA33/66 IDE CONNECTORS	
Size C	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 15 of 23	



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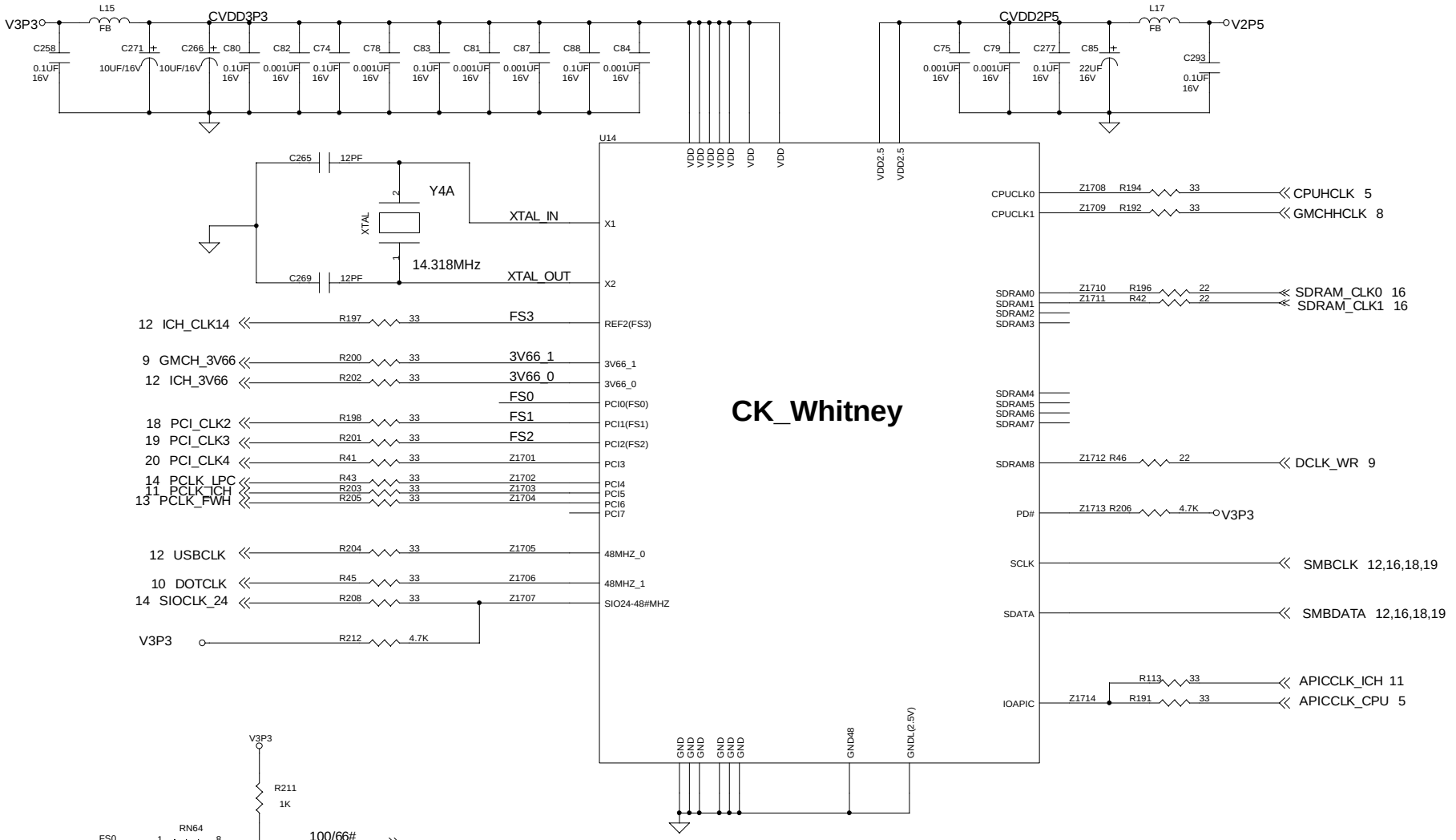
Title	Value Communications Appliance Reference Schematics SO-DIMM Interface	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 16 of 23	

Clock Synthesizer



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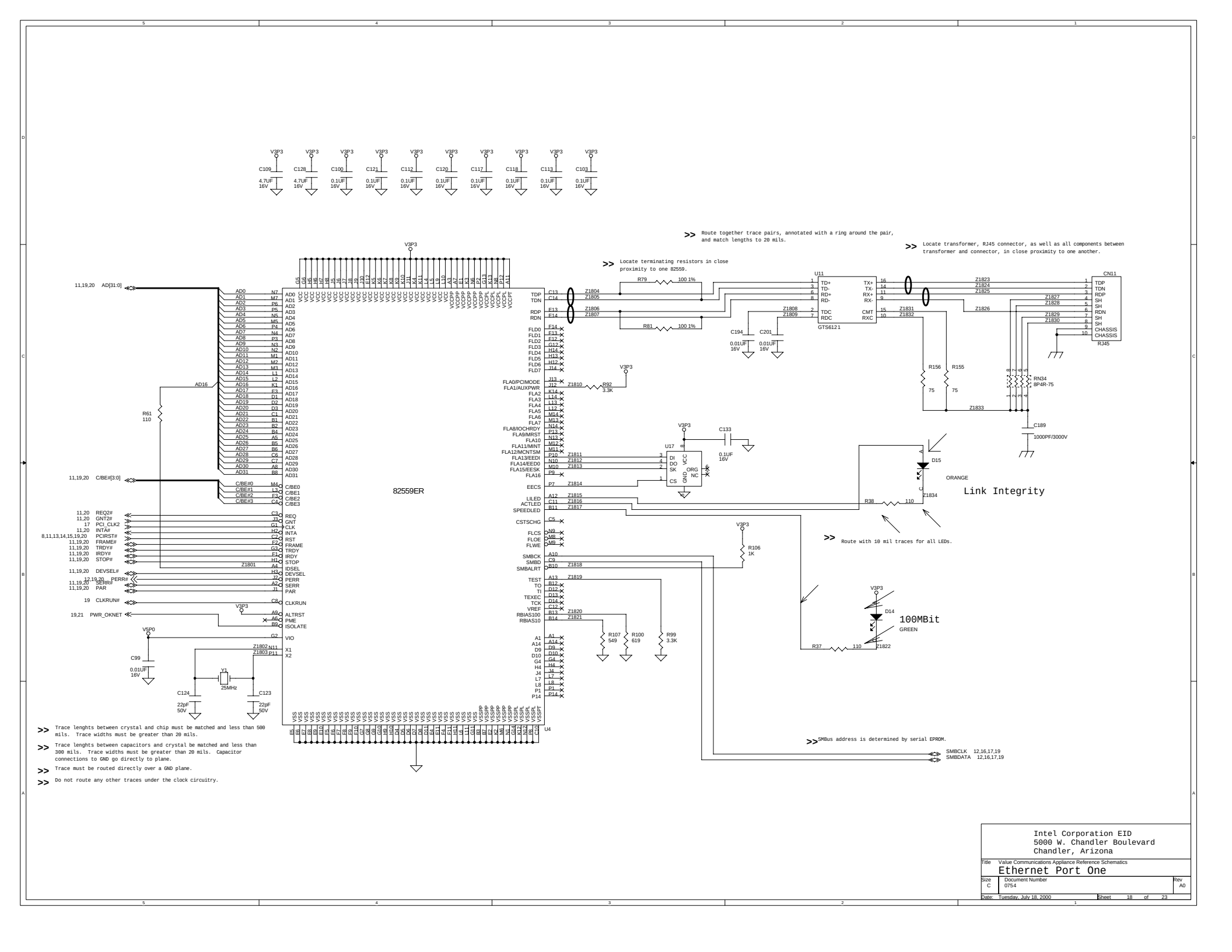
Title	Value Communications Appliance Reference Schematics Clock Generator	
Size B	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 17 of 23	


82559ER
GTS6121
RJ45
CN11
U11
U17
U4
RN34
8P4R-75
Link Integrity
100MBit
GREEN
ORANGE
Ethernet Port One
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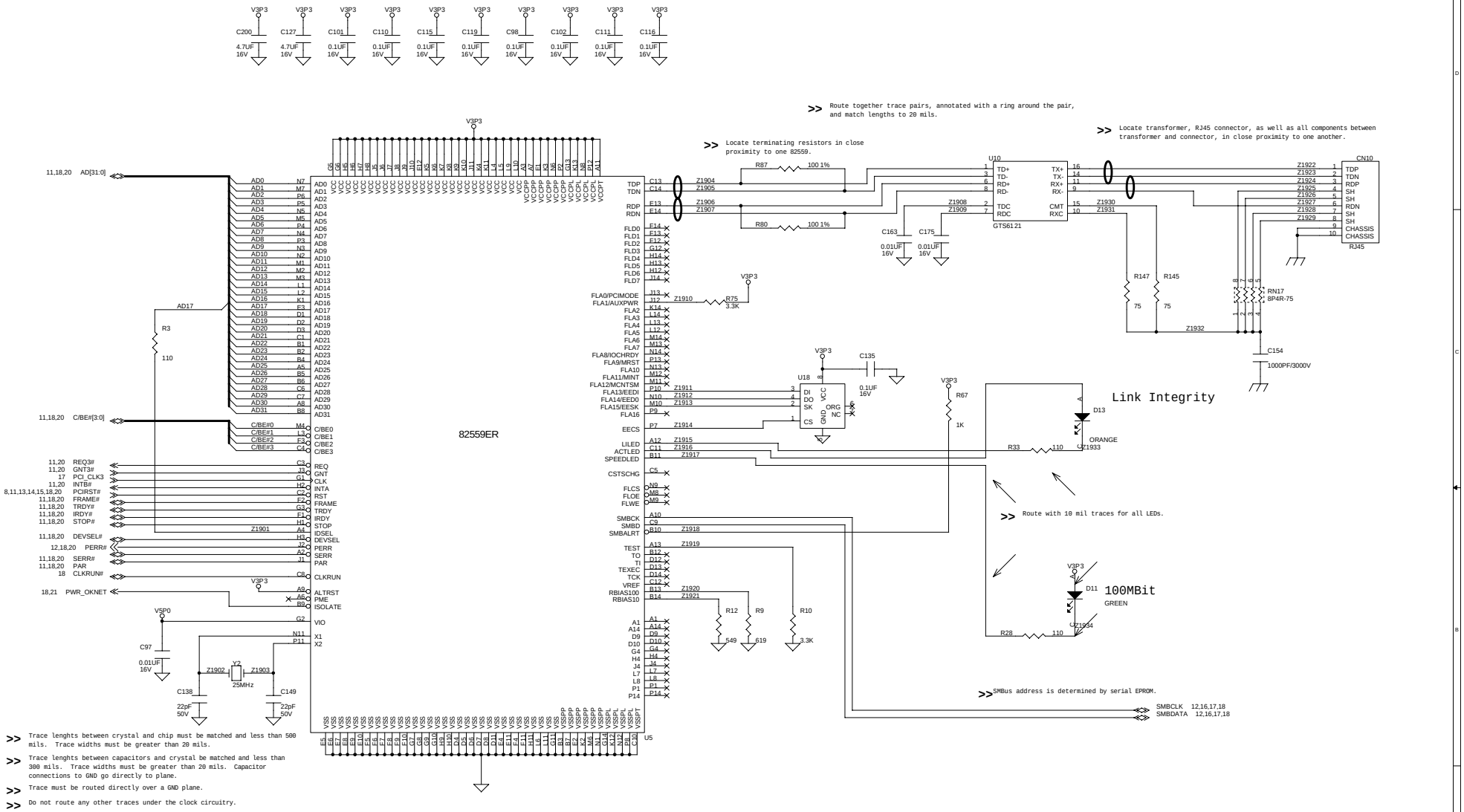
Chandler, Arizona
Value Communications Appliance Reference Schematics
Document Number 0754
Rev A0
Tuesday, July 18, 2000
Sheet 18 of 23



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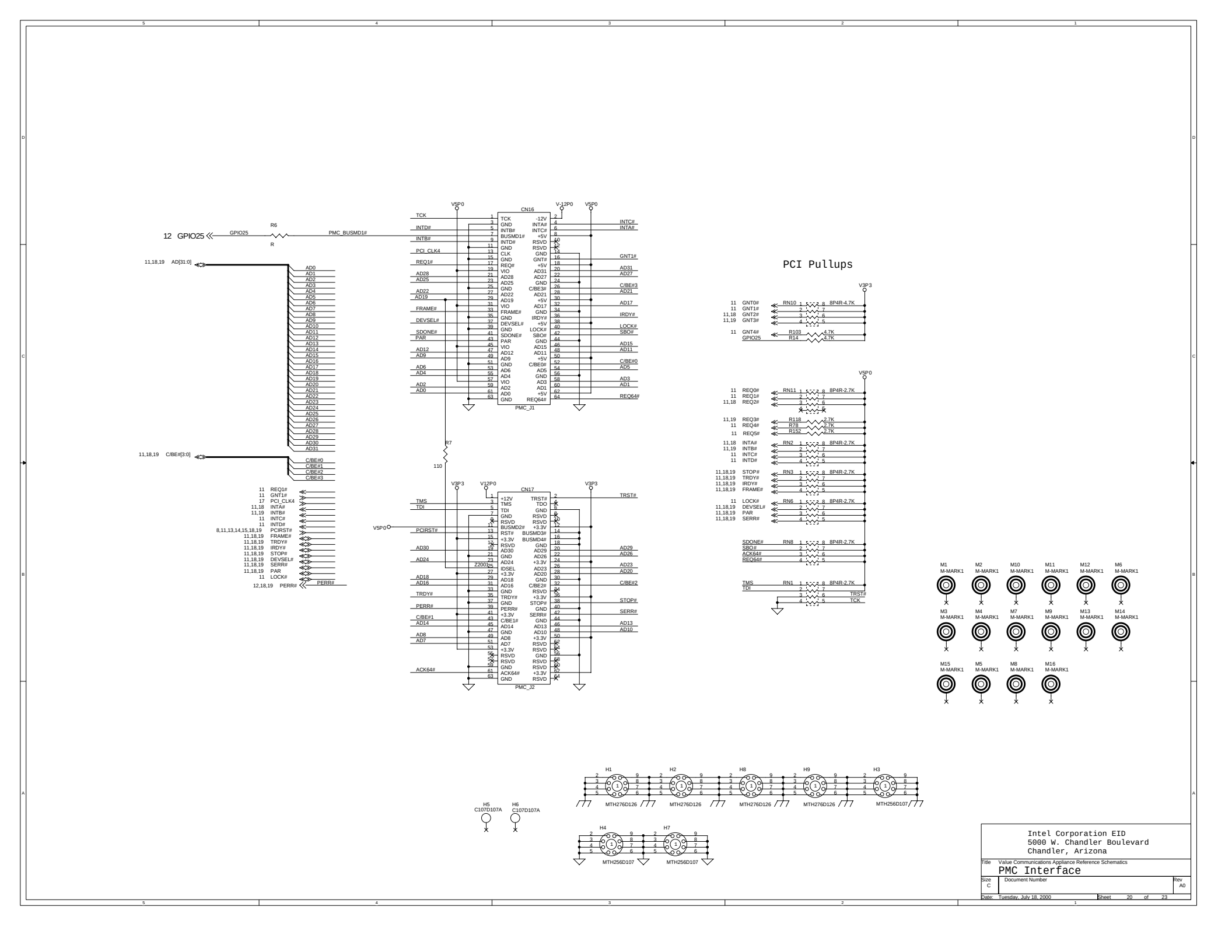
Title	Value Communications Appliance Reference Schematics
	Ethernet Port Two
Size: C	Document Number: 0754
Rev: A0	
Date: Tuesday, July 18, 2000	Sheet 19 of 23



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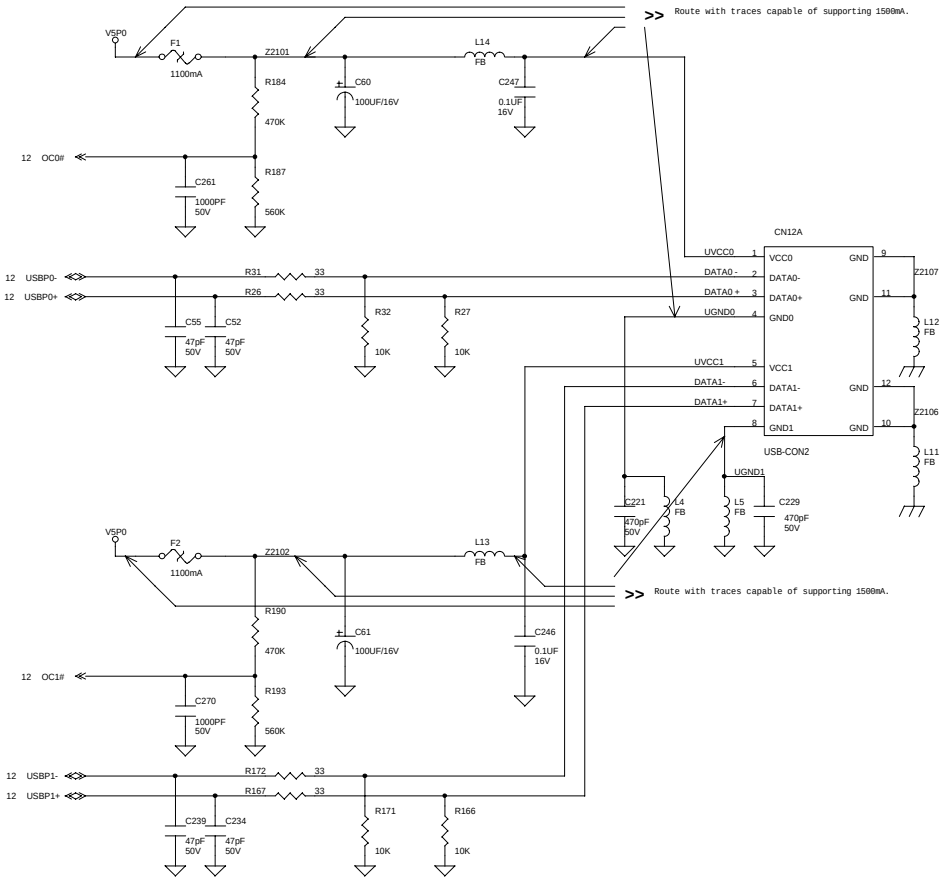
Title: Value Communications Appliance Reference Schematics

PMC Interface

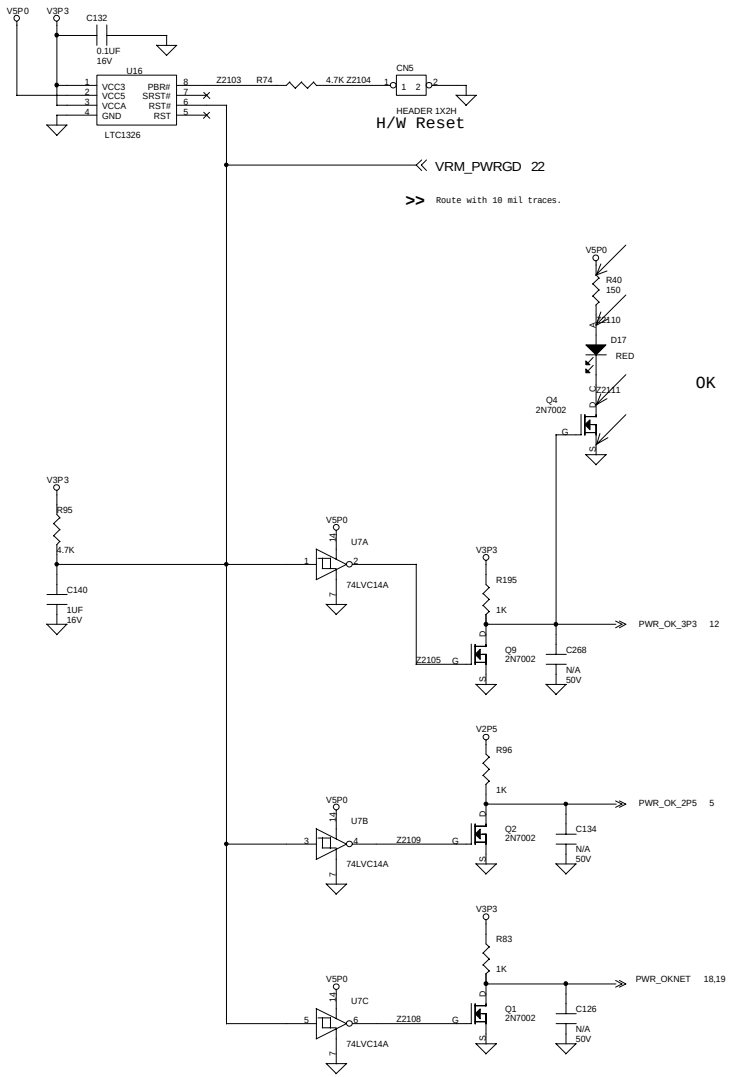
Size	Document Number	Rev
C		A0

Date: Tuesday, July 18, 2000 Sheet 20 of 23

USB CIRCUITRY



RESET CIRCUITRY



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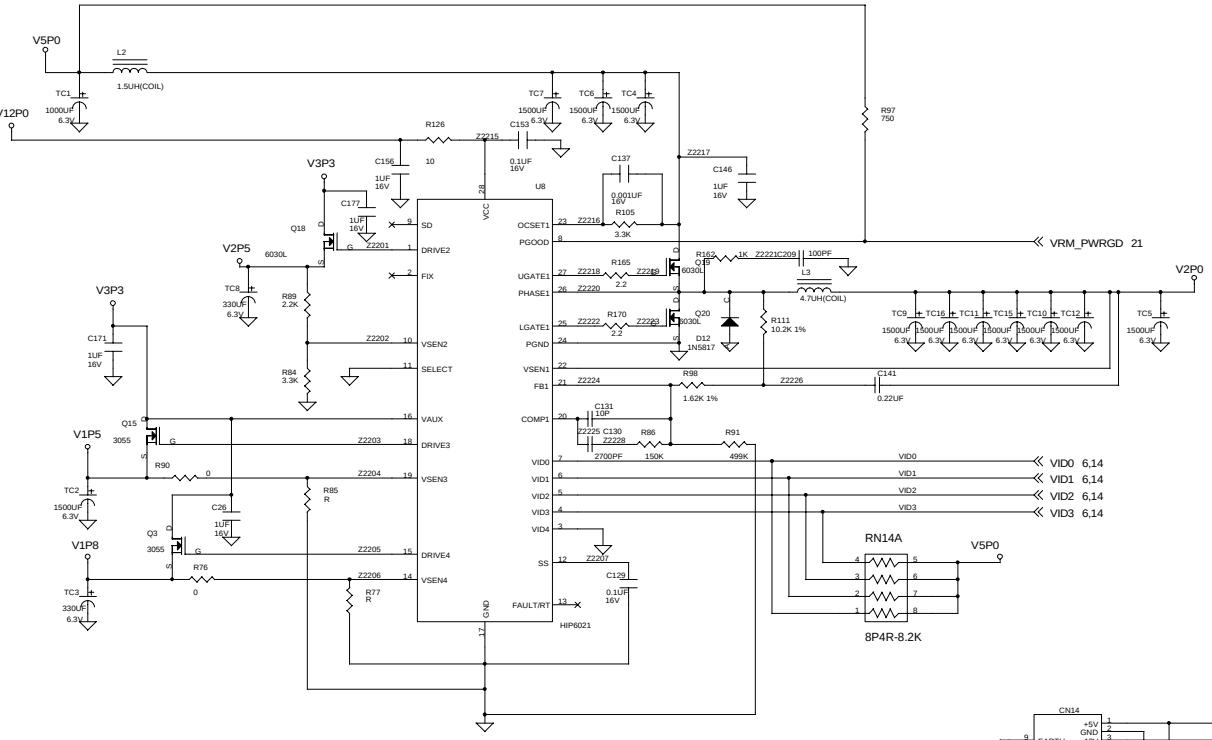
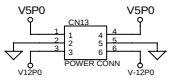
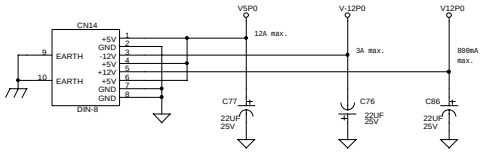
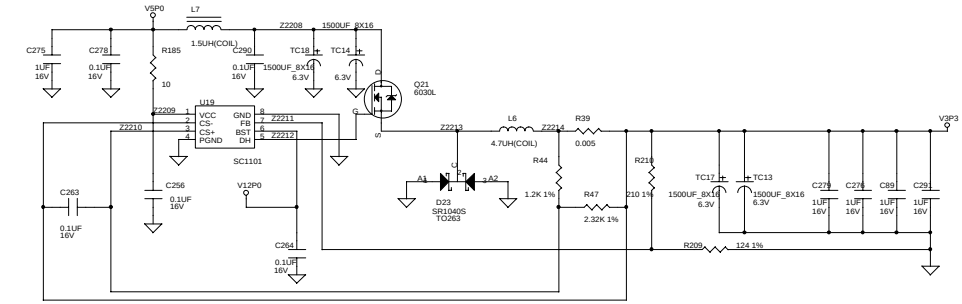
Title	Value Communications Appliance Reference Schematics Reset & USB Interface	
Size C	Document Number 0754	Rev A0
Date: Tuesday, July 18, 2000	Sheet 21 of 23	

VRM 8.4



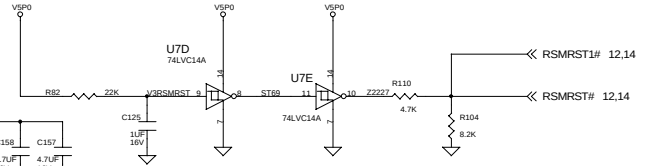


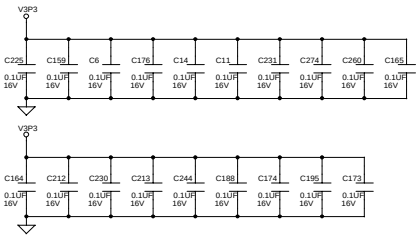


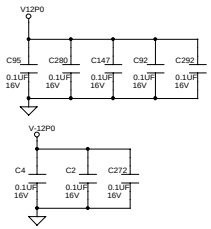


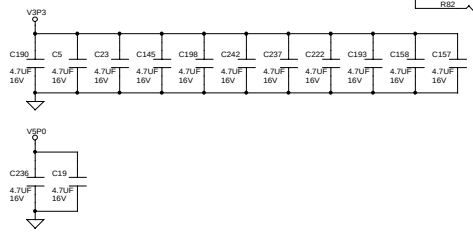
Resume Reset Circuitry

Schmitt Trigger Logic
using a 22msec delay









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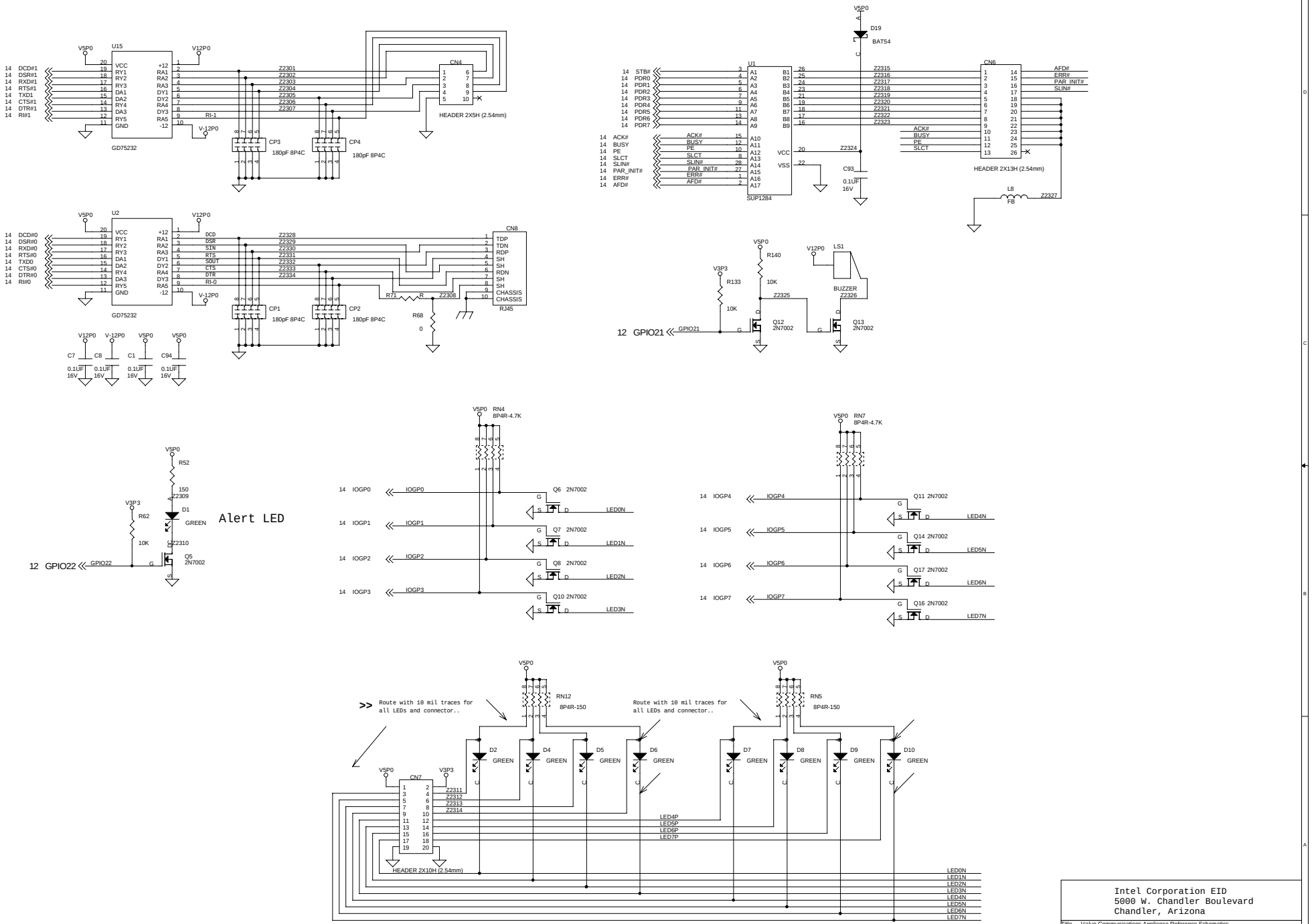
Size: Custom	Document Number: 0754 — Rev: A0
Date: Tuesday, July 18, 2000	Sheet 22 of 23



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FLASH, & Serial/Parallel Ports

Size	Document Number	Rev
C	0754	A0

Date: Tuesday, July 18, 2000 Sheet 23 of 23